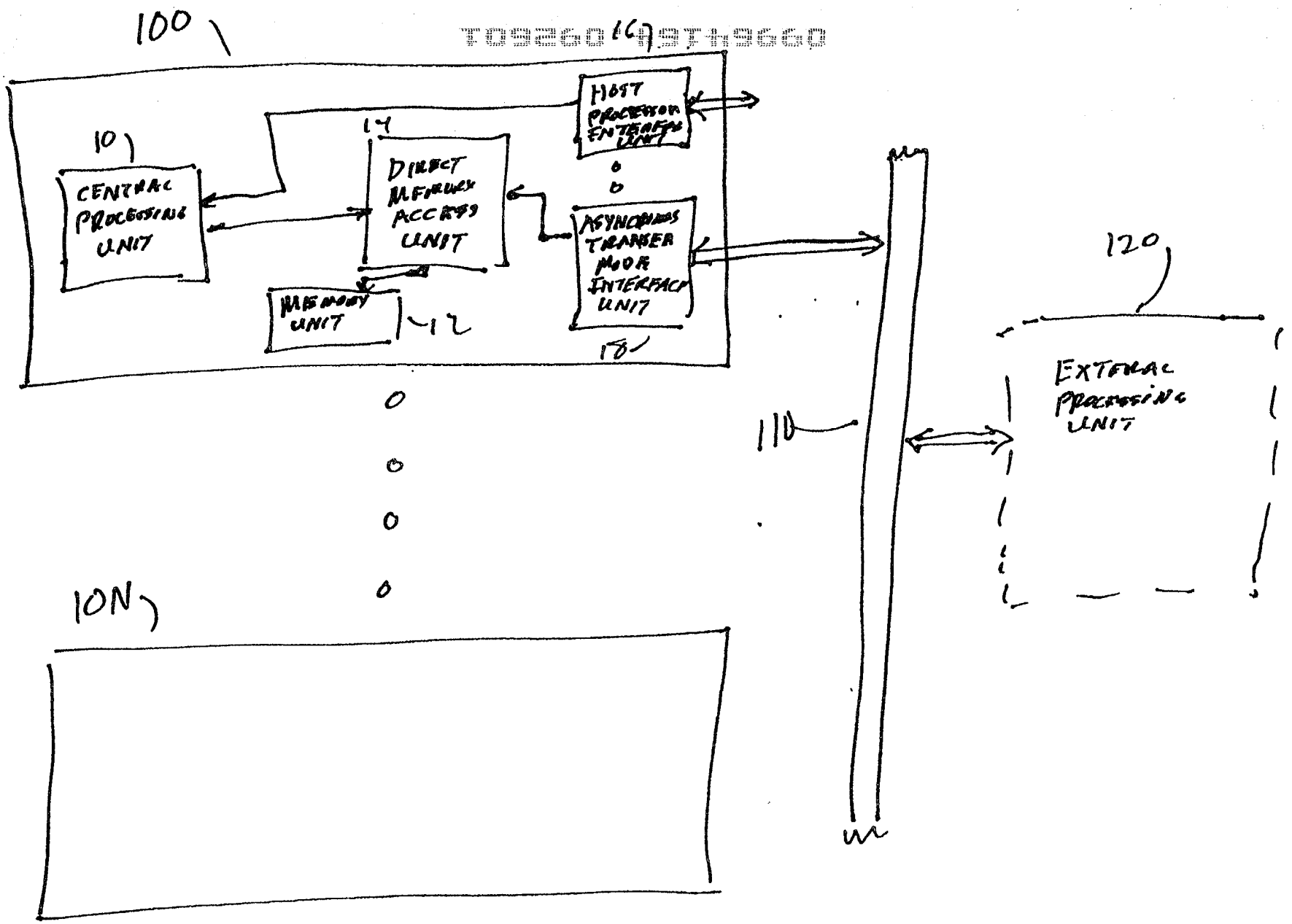

Fig. 1

TI-33533

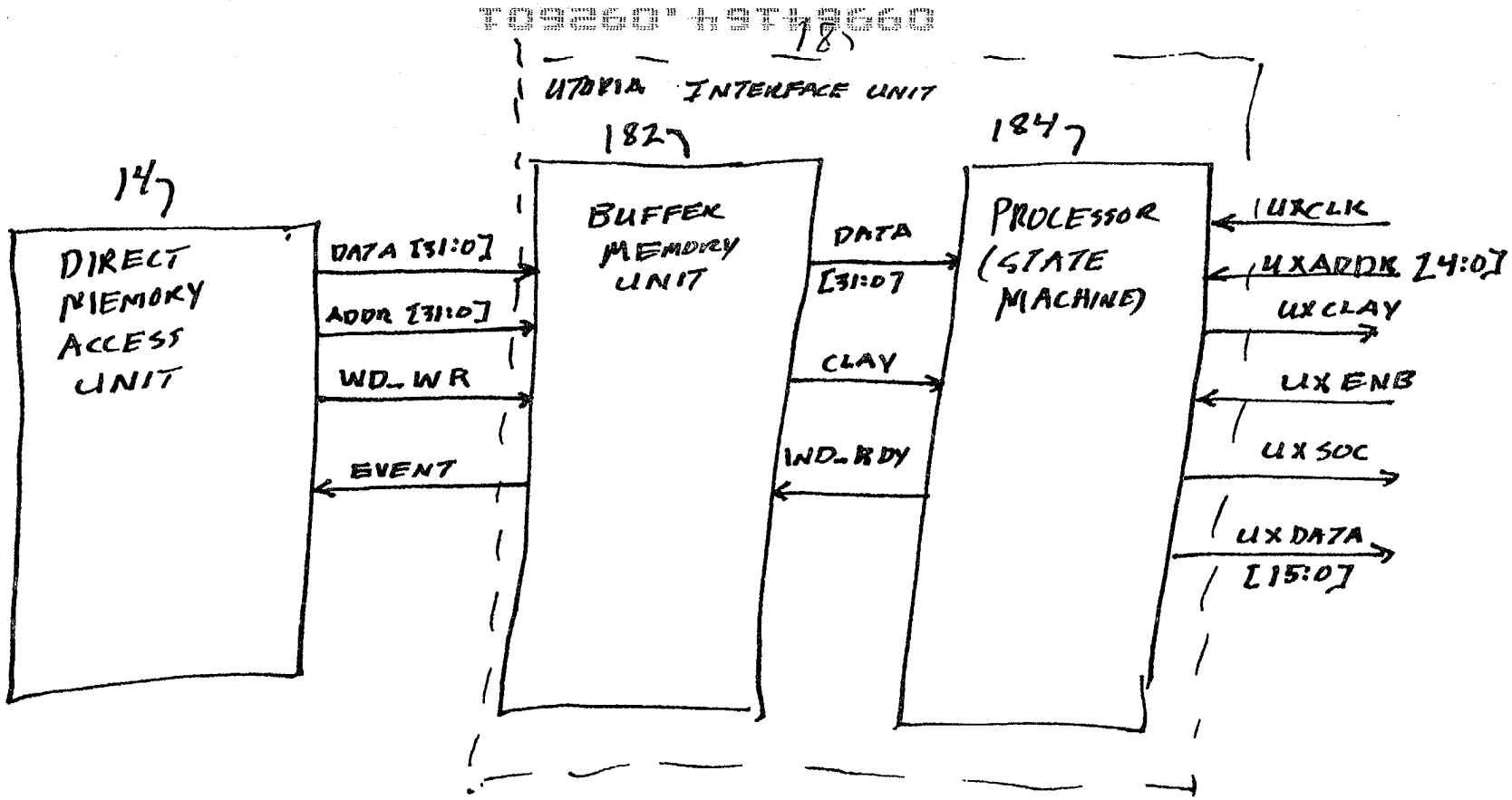
18
UTOPIA INTERFACE UNIT
14
DIRECT MEMORY ACCESS UNIT
182
BUFFER MEMORY UNIT
184
PROCESSOR (STATE MACHINE)
DATA [31:0]
ADDR [31:0]
WD_WR
EVENT
DATA [31:0]
CLAY
WD_RDY
UXCLK
UXADDR [4:0]
UXCLAY
UXENB
UXSOC
UXDATA [15:0]

Fig. 2

TI9260 "ISTA960

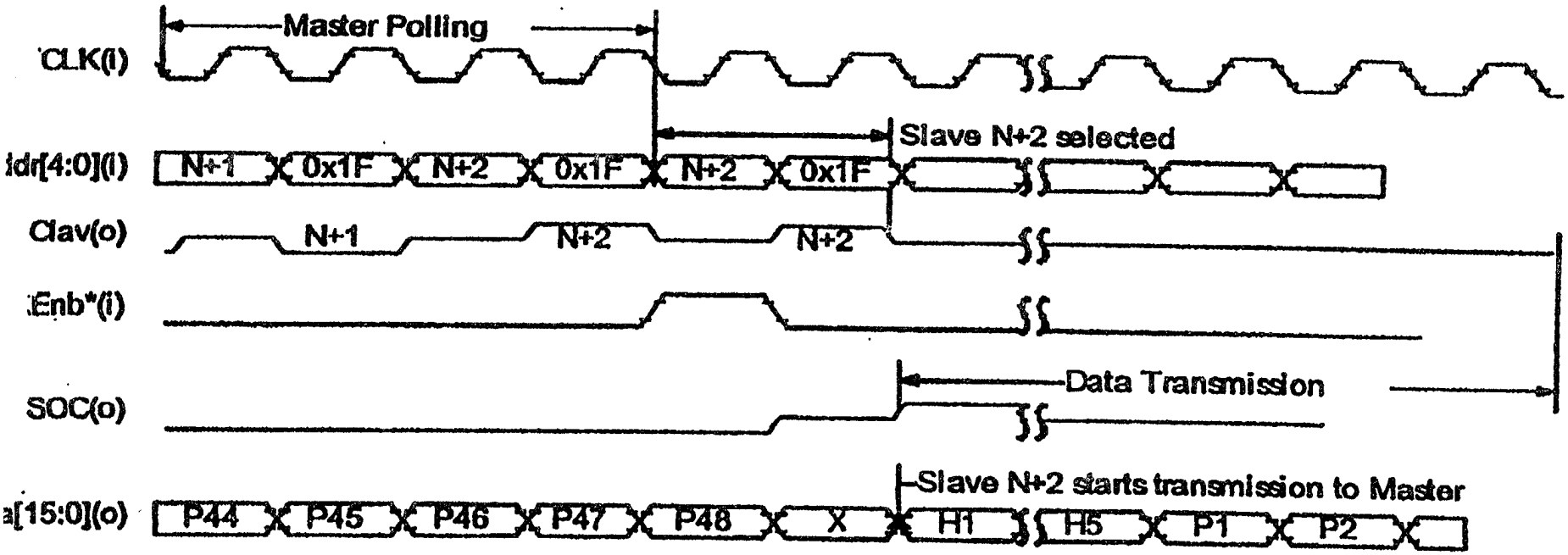

Fig. 3

TI-33533

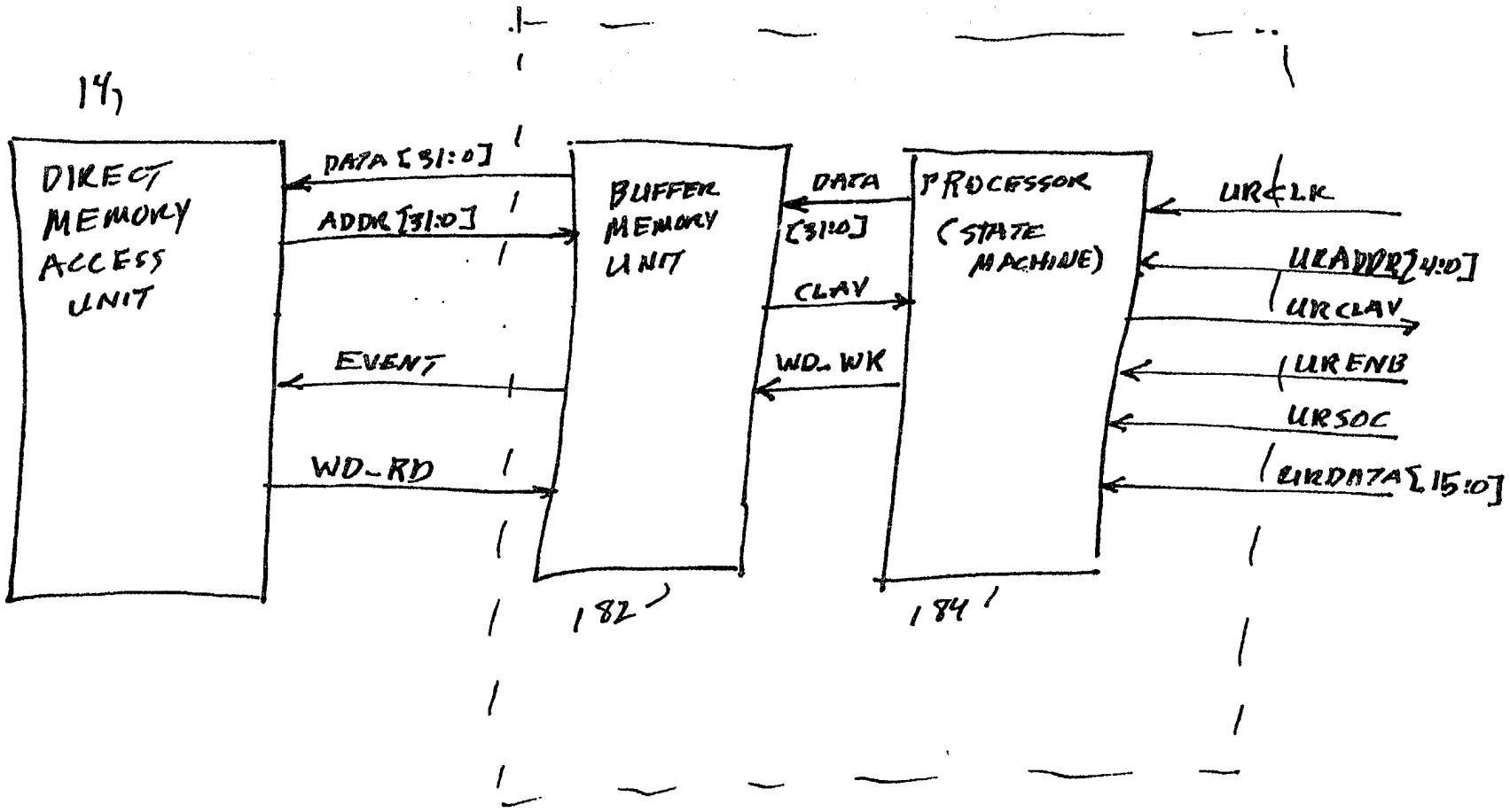

Fig. 4

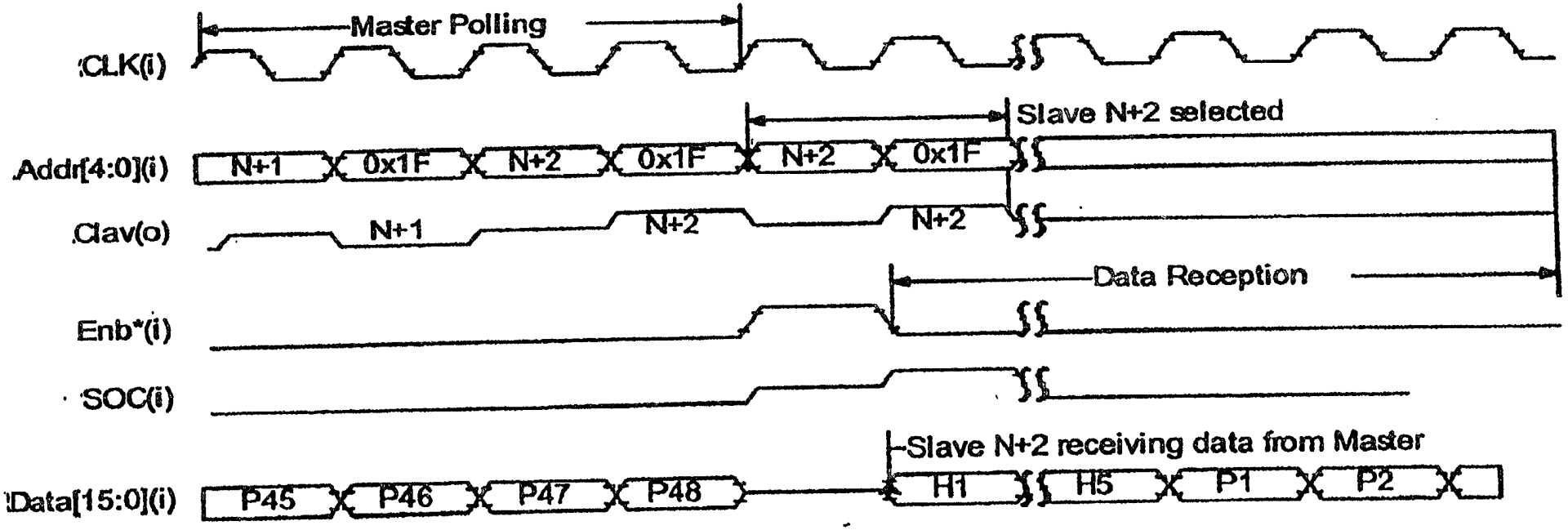
Master Polling
CLK(i)
Slave N+2 selected
Addr[4:0](i)
N+1
0x1F
N+2
0x1F
N+2
0x1F
Clav(o)
N+1
N+2
N+2
Data Reception
Enb*(i)
SOC(i)
Slave N+2 receiving data from Master
Data[15:0](i)
P45
P46
P47
P48
H1
H5
P1
P2

Fig. 5

TI9260 "9T"9660

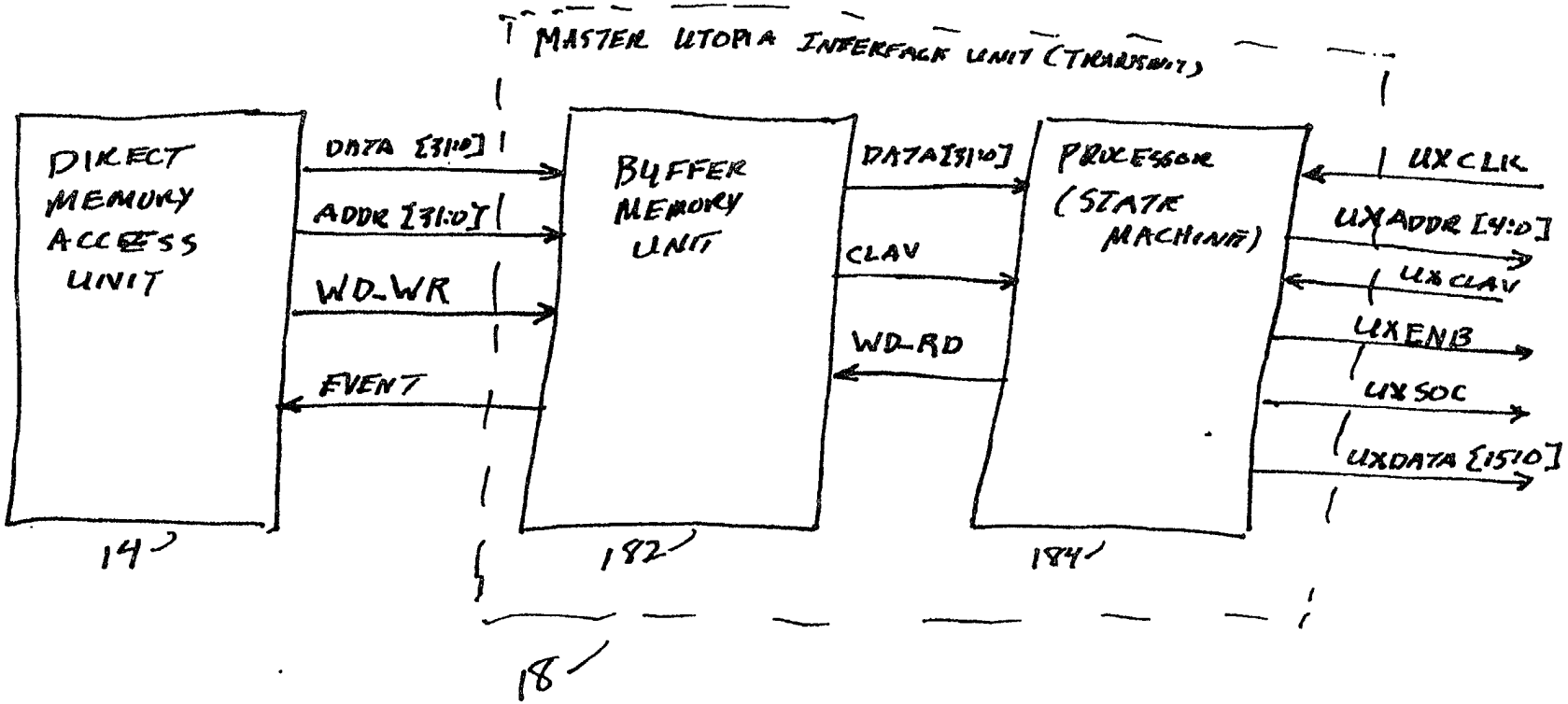

Fig. 6

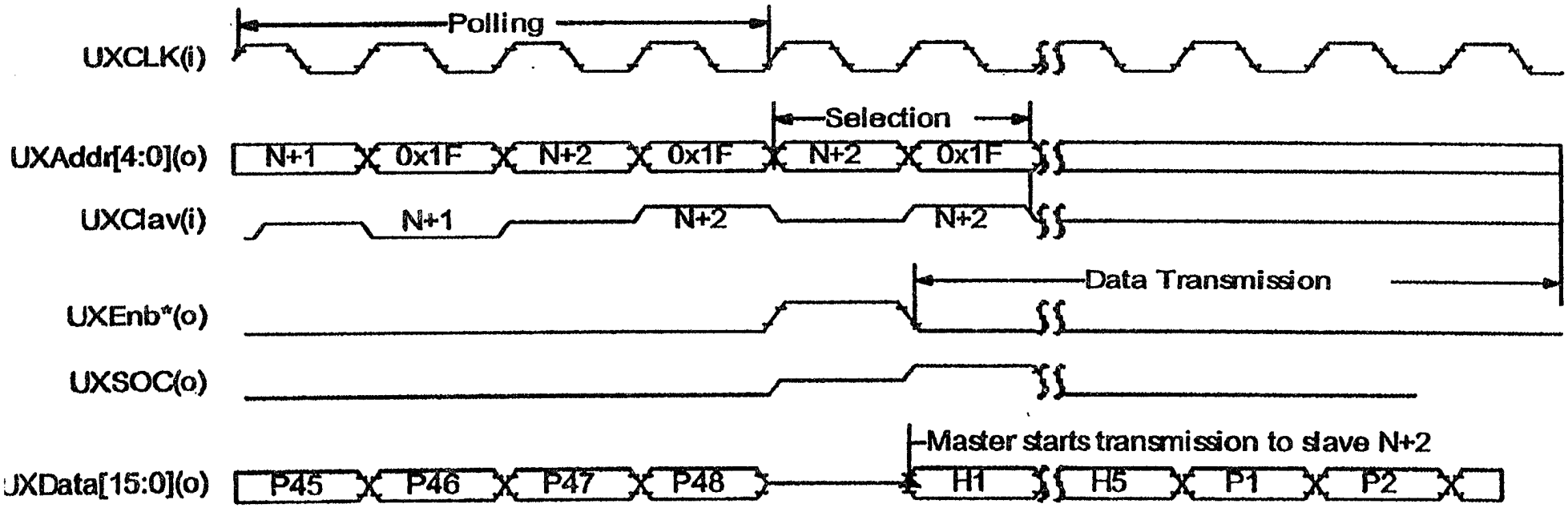
Polling
UXCLK(i)
Selection
UXAddr[4:0](o)
N+1
0x1F
N+2
0x1F
N+2
0x1F
UXClav(i)
N+1
N+2
N+2
Data Transmission
UXEnb*(o)
UXSOC(o)
Master starts transmission to slave N+2
UXData[15:0](o)
P45
P46
P47
P48
H1
H5
P1
P2

Fig. 7

T09260 "HATH9660

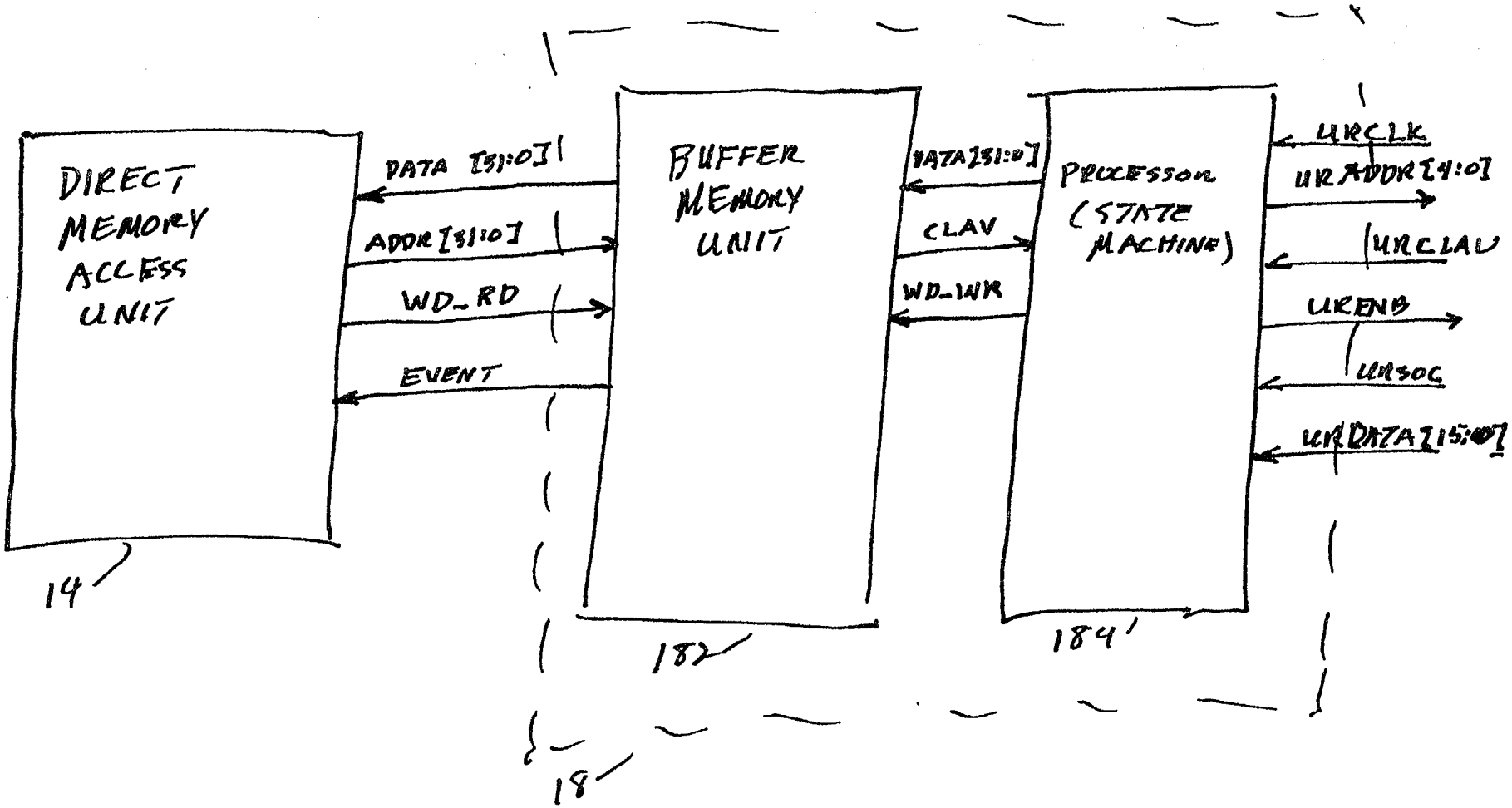

Fig. 8

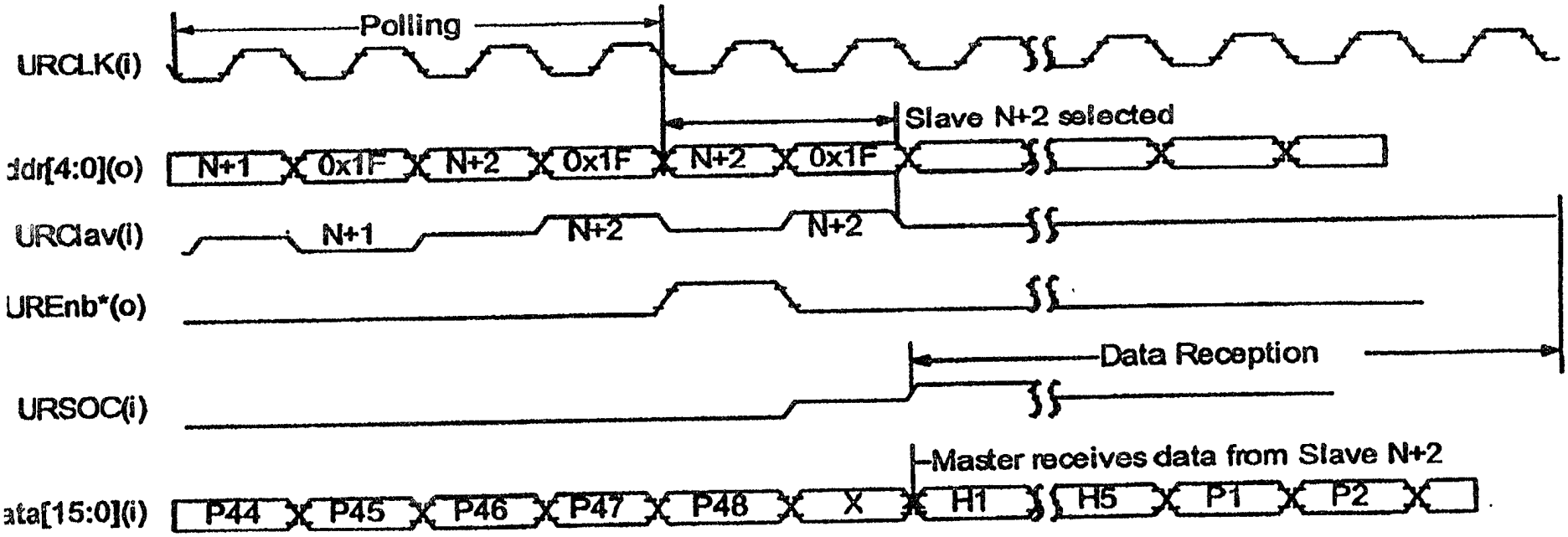

Fig. 9

TI-33533

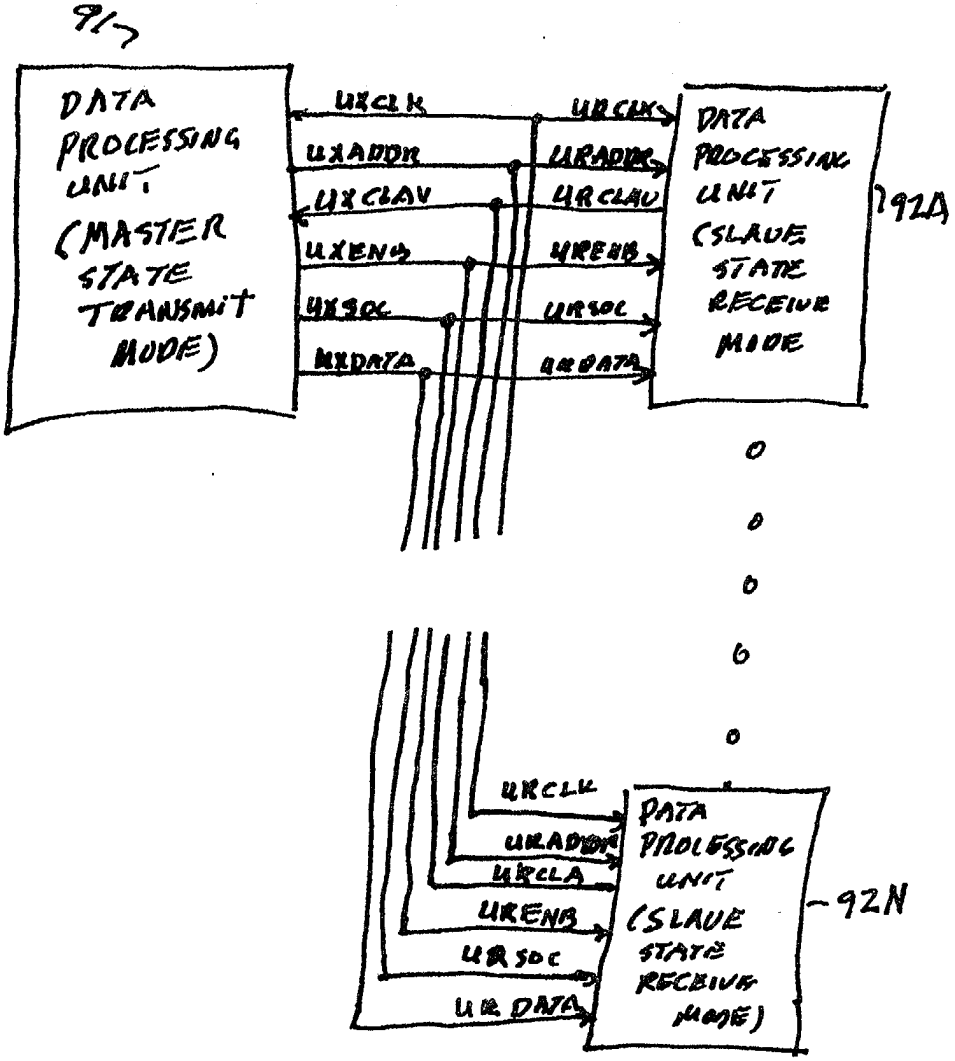

Fig. 10A

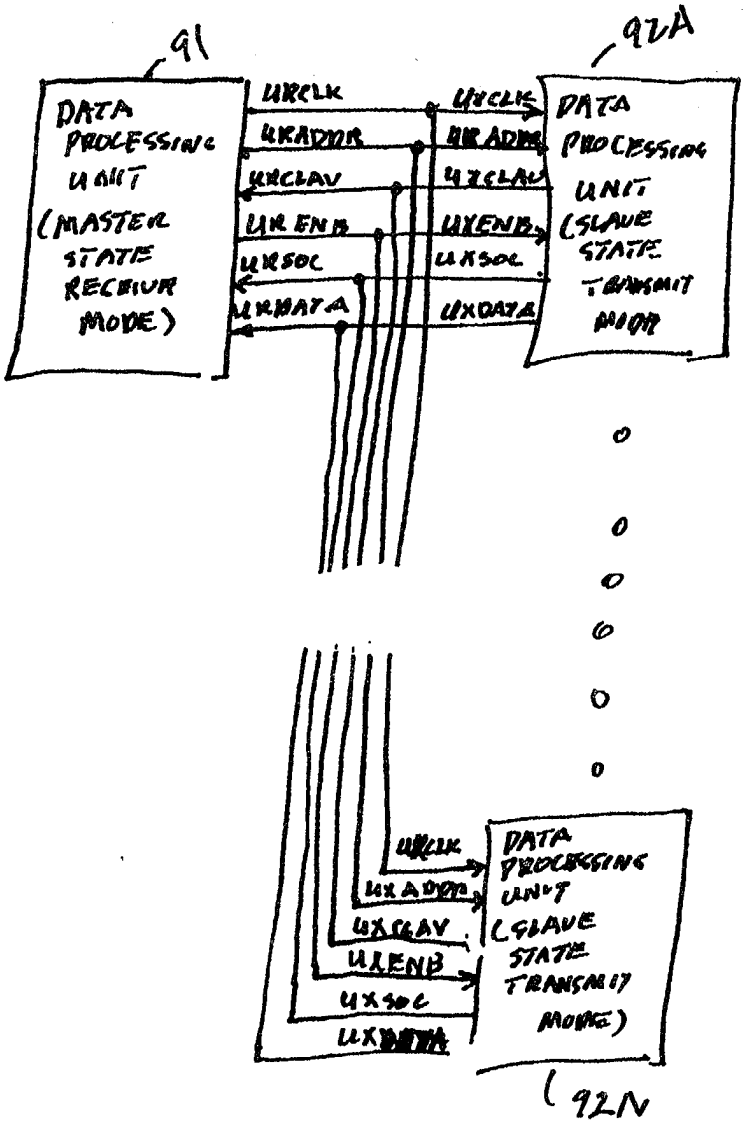

Fig. 10B

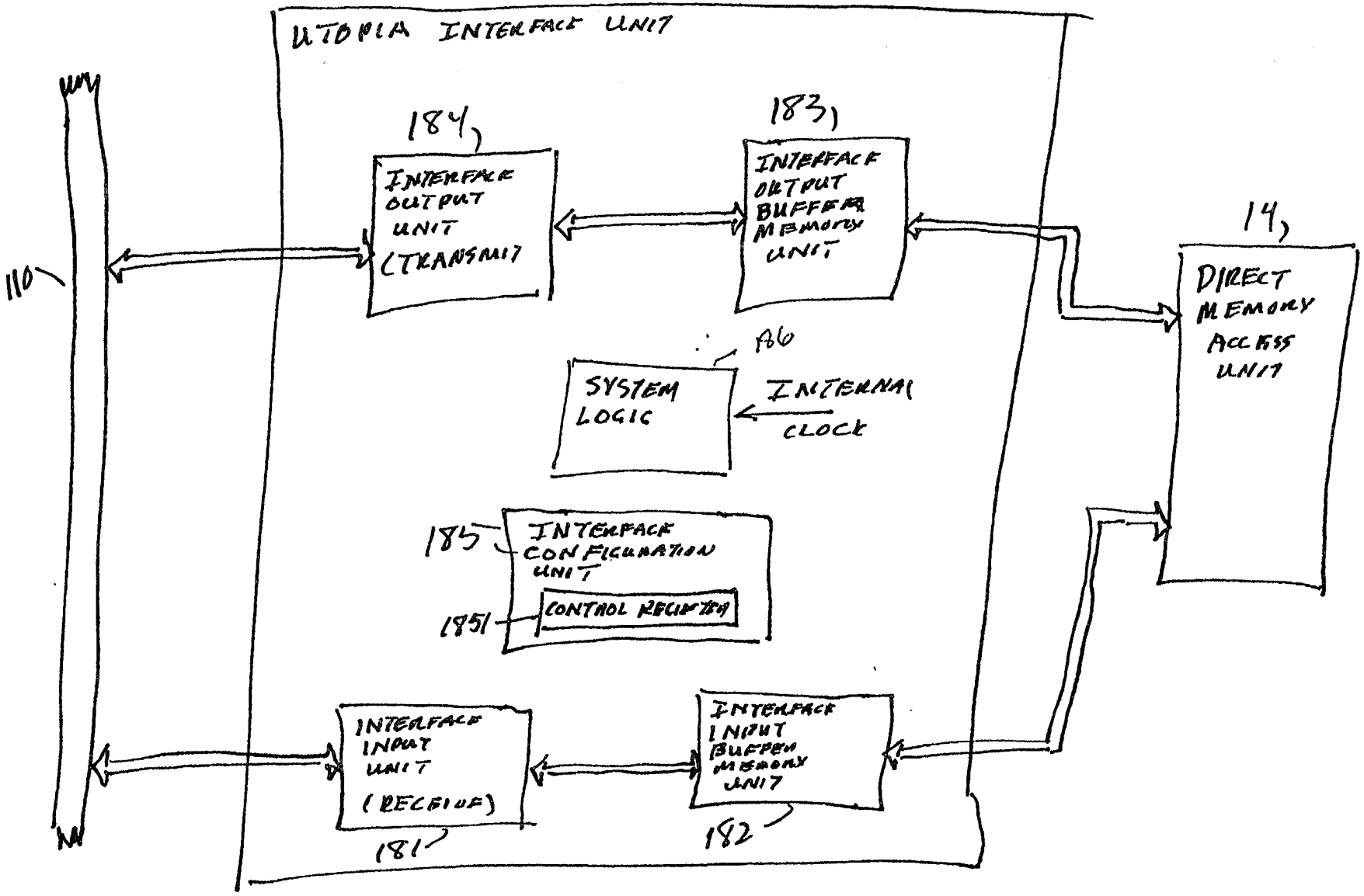

Fig. 11

TI-33533

31	30	29	28:24	23:22	21:18	17	16
END	Rsv	Rsv	SLID / SLEND	Rsv	XUDC	UXMSTR	UXEN

15	14	13	12	11:10	9:8	7:6	5:2	1	0
JLB	MPHY	U16M	UPM	Rsv	Rsv	rsv	RUDC	URMSTR	UREN

Fig. 12

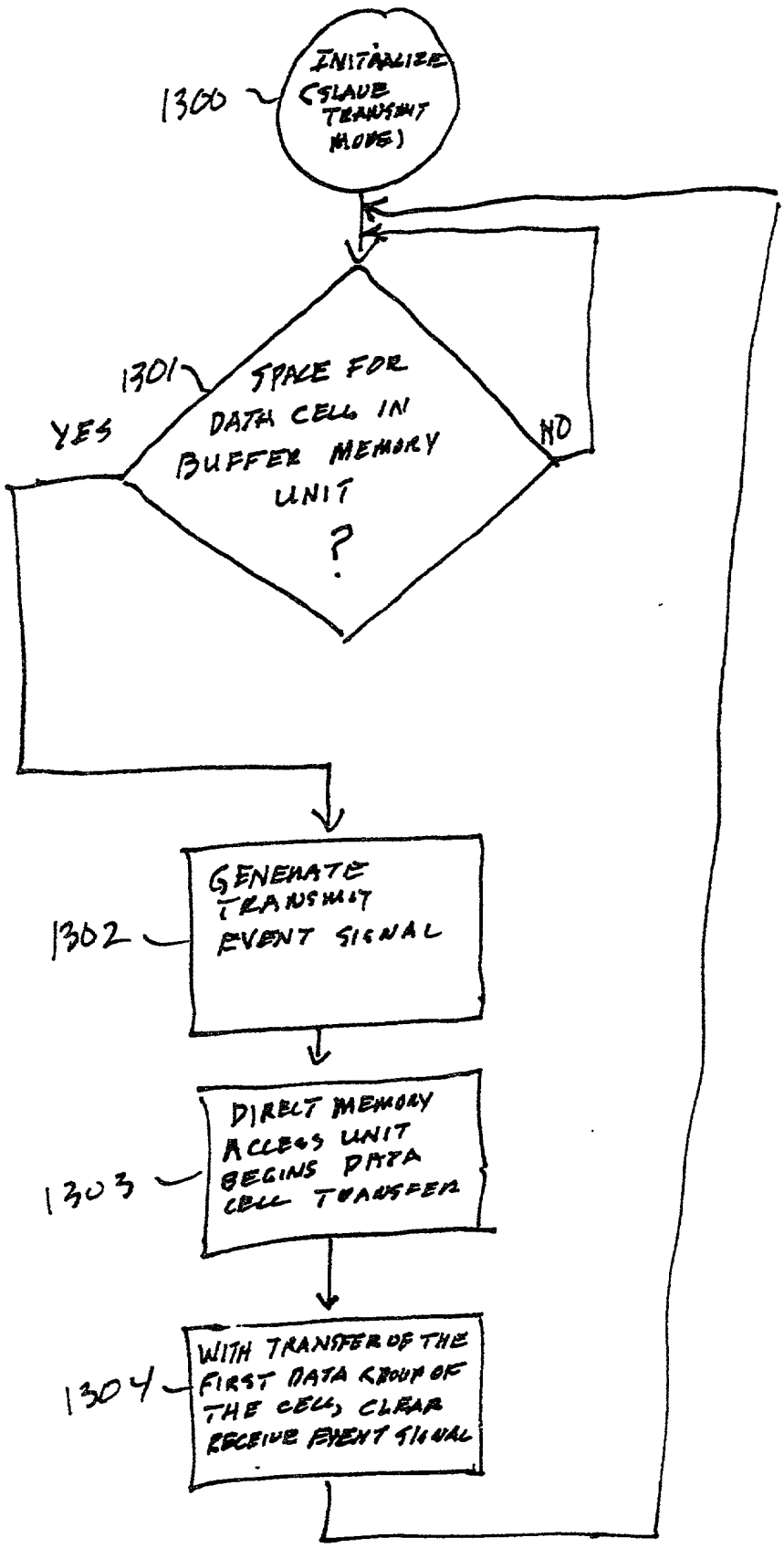

Fig. 13

TI-33533

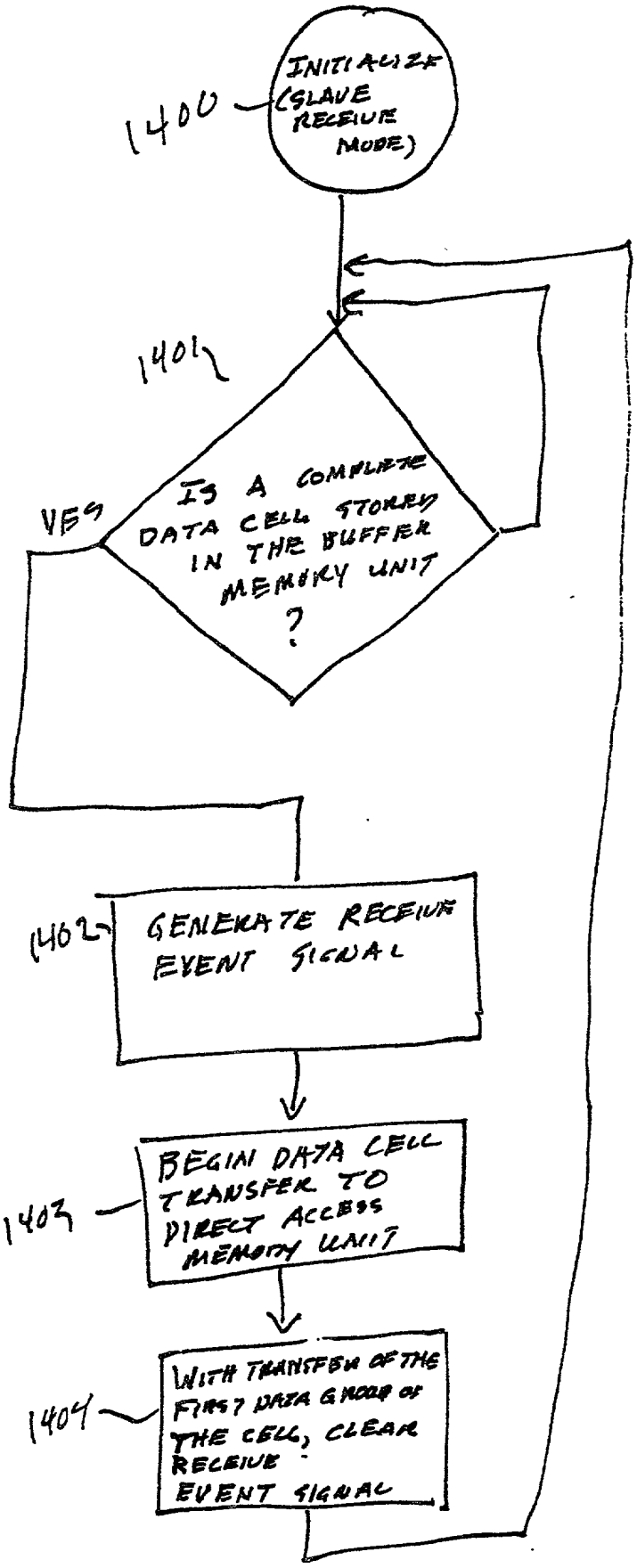

Fig. 14

TI-33533

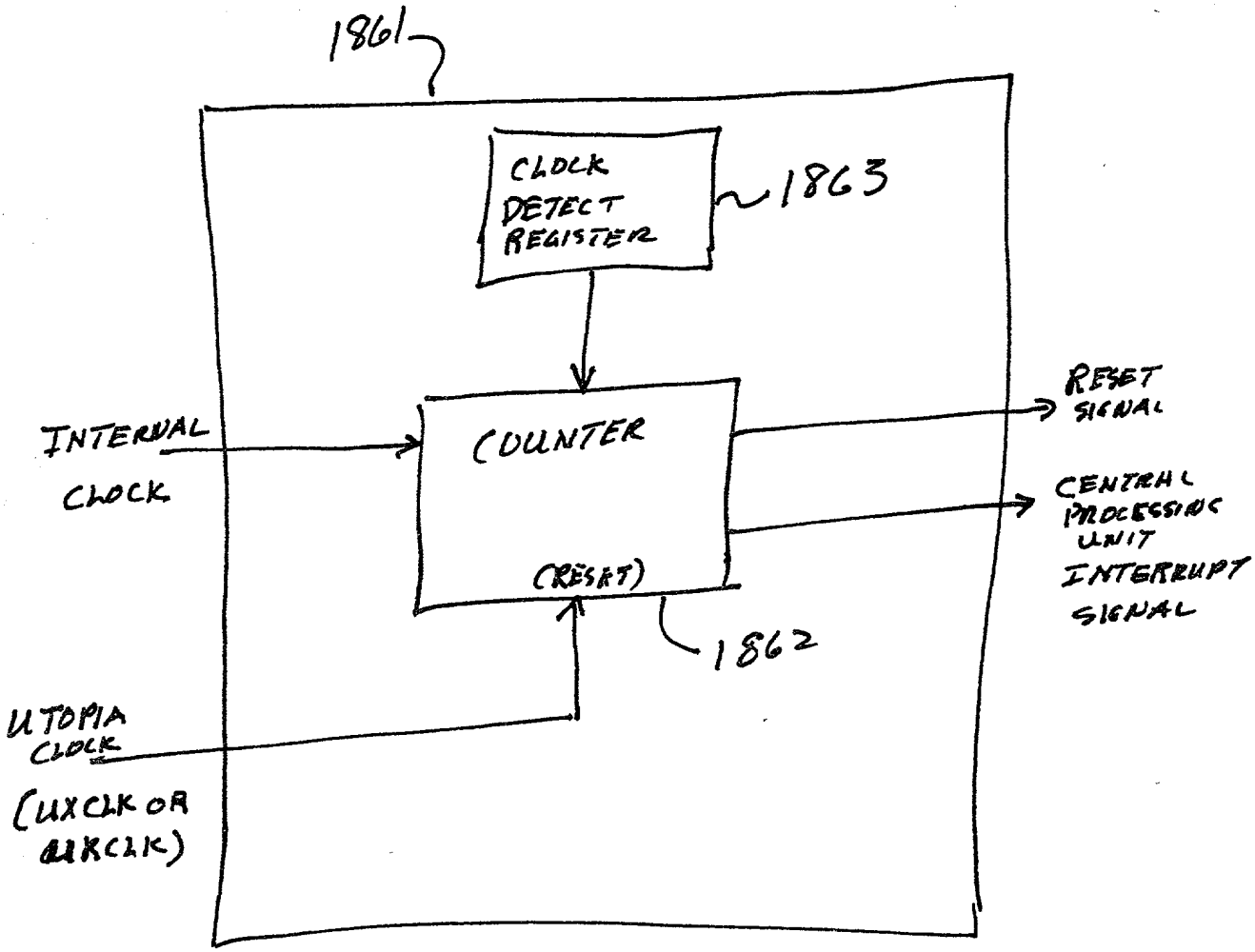

Fig. 15

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